IN THE SPECIFICATION

Please amend page 21, 1st and 3rd paragraphs as follows:

Referring to Figure 2a and ~~Figure2b~~ Figure 2b each FFT channelizer 310 comprises an input high-speed data port 307 and DMA buffer 308 connected to the FFT device 310 composed of three parallel FFT engines FFT1 - FFT3, with complex spectral output collected by DMA buffer 330 and distributed by a high-speed data router port 370. The high-speed data router port 370 is connected to a respective high-speed data router port 407' of first channel processor 410' of signal processing module 40, and if configured by the high-speed data router, to a second high-speed data router port channel processor 407". If the data router 370 of the channelizer module 30 configures both first and second channel processors, the first channel processor 410□ receives the upper half of FFT channelizer complex spectra segments outputted from a corresponding FFT channelizer 310, while the second channel processor 410" receives the lower half of the FFT channelizer complex spectra segments.

Each respective FFT unit 310 performs an N-point complex FFT transformation using a block of complex signal data contained in the DMA buffer 308. Referring to ~~Figure2b~~ Figure 2b, the operation of the three FFT units comprising FFT unit 310 is orchestrated in time such that there is an overlap in data used by the first and second FFT units, the second and third FFT units, and in a cyclic manner, the third and first FFT units. In the embodiment of the preferred invention, the overlap is 12.5 percent. However, the device is not limited to such specific overlap values, and other overlaps such as 25 percent may be used.